Astronics Test Systems Inc.



Key Features

- IP 1553 bus
- 64 channels for temperature or pressure
- Frequency counter
- 48 TTL inputs
- 32 TTL outputs
- 16 open drain outputs
- On-board D/A converter
- Nonvolatile memory
- · 60 updates/s



The Trig-Tek[™] 260B Multi-Function Unit is designed for applications requiring up to 80 channels of digital I/O and for observing and/or recording 16 to 64 channels of pressure or temperature.

Product Information

The 260B consists of a motherboard that connects up to four daughterboards to the IP 1553 serial bus.

Each of the modules has 16 pressure or temperature channels, a frequency counter, 12 TTL digital input channels, eight TTL output channels, and four open-drain outputs with 2 A current capability.

Each module has both nonvolatile memory to store zero and gain coefficients as required to calibrate the channels and an on-board Digital-to-Analog (D/A) converter to generate accurate DC voltages for calibration. The modules include an RS232 bus for updating the flash to install new firmware changes.

The serial data from the four modules is time division multiplexed, assembled, and delivered to the bus with a 60 updates/s rate.



Specifications

Note: The Astronics Test Systems policy is one of continuous development and improvement. Consequently, the equipment may vary in detail from the description and specifications in this publication.

Motherboard Assembly

Included in the motherboard are the reference voltages and the logic to interface up to four daughterboards to the IP 1553 Serial Bus.

Reference Voltages

- Reference Voltages: +5.00 V, -5.00 V, and +10.00 V
- All the reference voltages are derived from the same high-precision 5.00 V reference.
- It has an adjustment to set the voltage level.
- It has a 10 PPM/° C temperature coefficient.
- The three reference voltages are distributed via the interface connectors to the daughterboards.

Logic

- The motherboard uses a 16-bit micro controller to provide time division multiplexing to interface up to four daughterboards to the IP 1553 Serial Bus with a 60 updates/s rate.
- The IP 1553 bus resides on the motherboard.

IP 1553 Data Bus Interface

Connectors

• Two triaxial BNC connectors marked "J8" for Ch A and "J7" for Ch B

Interface

Power

• 18 to 36 VDC @ 125 mA Current

Environmental

Operating Temperature

 \bullet -10° to 70° C

Storage Temperature

 \bullet -40° to 85° C

Mechanical

Dimensions

• 14" H x 10" W x 1.25" D

Connectors

- TB1: A 3-Pin terminal strip marked "TB1" with "28 V," "RET" (return), and "CHS" (chassis ground)
- TB2: A 3-Pin terminal strip marked "TB2" with "+5" (5 V @ 250 mA), "RST" (microprocessor reset), and "DG" (digital ground)

Daughterboard Assembly

Up to four daughterboards will interconnect with a motherboard to interface with the IP 1553 Serial Bus.

The daughterboards have nonvolatile memory for storing the offsets and gain coefficients for each channel.

Data Inputs

(16 Channels)

Impedance

• >50 MΩ

- Input Level
- Gain: 1
- -10 V to +10 VDC
- Gain: 10 -1 V to +1 VDC
- Gain: 100 -0.1 V to +0.1 VDC

DC Offset vs. Temp

• ±1 µv/° C

Gain

• 1, 10, 100, ±0.05%

A/D Reading Accuracy

- Accumulative Offset Error: 12 mV (adjustable to Zero)
- Accumulative Gain Error: 0.6% FS (adjustable to ±1 LSB)

Linearity

• ±2 LSB

Open Thermocouple Detection

 -1.00 ±0.05 V indication (with the gain of 100)

Over Voltage Protection

Up to 40 V

Adjacent Channel Isolation

• >76 dB

Connector

 The 32 pins of a 64-Pin terminal strip marked "-DATA+"

Note:

 Analog outputs are multiplexed into a 16-bit analog to digital converter. The digital data is placed on the DATA bus.

Trig-Tek[™] **260B**

Frequency Input (1 each)

Impedance

• >200 k Ω

Frequency Range

• 1 Hz to 5 kHz

Accuracy

• Reading ±0.05 Hz (±3 RPM)

Wave Form

- Sine, Square, Triangle, or Pulse (pulse width >40 $\mu s)$

Level

• 50 mV to 200 V_{pk-pk}

Connector

 The terminal strip is marked "Freq Input." The top two terminals are marked "-SIG+" for signal input. The lower two terminals are marked "-EXC+" (+5 V excitation) and "DG" (digital ground).

Digital Input

(12 each)

Function

TTL Logic

Impedance

• >470 k Ω

Input Protection

• >50 V

Connector

• The terminal strip is marked "TTL Inputs." The top 12 terminals are signal; the lower 12 are DG.

Excitation Outputs

(16 channels)

Impedance

• <0.1 Ω

Level

• 5.00 VDC, ±20 mA

Current

 Short circuit protected above 100 mA each channel

Connector

 The 32 pins of a 64-Pin terminal strip marked "-EXC +"

Cold Junction

LM35 RTD Temperature Repeatability

• ±0.5° C

Specifications

continued

D to A Outputs

(X1 and X.01)

- Impedance < 50 Ω

X1 Level

-10 to +10 VDC

X.001 Level

-10 to +10 mVDC

Accuracy

Setting: ±0.05% of FS

Connectors

 These terminals are marked "X1-X.01 D/A Output." The top two terminals are signal; the lower two are COM.

Digital Outputs

(8 each)

Level

• 0 to 5 V

Source Current

• Up to 20 mA

Connectors

 These terminals are marked "TTL OUTPUTS" with channels 1 through 8 marked "Ch1," "Ch2," and so on. The top eight terminals are signal; the lower eight are DG.

FET Outputs (High Current)

(4 each)

Voltage

• Up to 60 V

Source Current

Up to 2 A

Ordering Information

TT6156 : Trig-Tek[™] 260B Multi-function Unit - motherboard

TT6092 : Trig-Tek[™] 260B

Multi-function Unit - daughterboard

Connector

· The top terminals four are source, and the lower four are drain (must be returned to DG)

Interface

Voltage

- Input Voltage Range: 18 to 36 VDC (unregulated)
- A 3-Pin terminal strip marked "28 V"

Current

· Daugherboard: 400 mA

Connector

 3-Pin terminals marked "28 V," "RET" (return), and "CHS" (chassis ground)

Environmental

Operating Temperature

-10° to 70° C

Storage Temperature

-40° to 85° C

Dimensions

 1.25" H x 10" W x 11" L (3.2 cm x 25.4 cm x 27.9 cm)

Open Drain Outputs

- The drain and source of the FET are brought out on terminals that are floating with respect to digital ground to which the gate is referenced. The purpose for floating the FET source is to assure that the solenoid power source has a proper return path, as the current may be up to 2 A.
- If the power source for the solenoid is floating, then the FET source must be connected to the digital ground at the board edge. This should be done by jumpering the source terminal to the ground terminal of an adjacent digital channel. If the power source ground is common with the digital ground, it will provide the source ground.

SOLENOID



Trig-Tek[™] **260B**

EE 1-POWER μC DIGITAL ADJACE SCHEMATIC **OPEN DRAIN PORT**